

Application No. 10/640369 (Docket: CNTR.2200)  
37 CFR 1.111 Amendment dated 12/02/2005  
Reply to Office Action of 09/02/2005

**AMENDMENTS TO THE CLAIMS**

Kindly amend claim 12 as shown in the following listing of claims. The listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims**

1. (Original) A non-inverting domino register, comprising:
  - a complementary pair of evaluation devices responsive to a clock signal;
  - evaluation logic, coupled between said complementary pair of evaluation devices at a pre-charged node, that evaluates a logic function based on at least one input data signal;
  - a storage stage driving a first preliminary output node, said storage stage comprising a first pull-up device and a first pull-down device both responsive to said pre-charged node, and a second pull-down device responsive to said clock signal;
  - a keeper circuit having an input coupled to said first preliminary output node and an output that drives a second preliminary output node; and
  - an output stage driving an output node, said output stage comprising a second pull-up device and a third pull-down device both responsive to said pre-charged node and a third pull-up device and a fourth pull-down device both responsive to said second preliminary output node.
2. (Original) The non-inverting domino register of claim 1, wherein said complementary pair of evaluation devices comprises:
  - a P-channel device having a gate receiving said clock signal and a drain and source coupled between a source voltage and said pre-charged node; and
  - an N-channel device having a gate receiving said clock signal and a drain and source coupled between said evaluation logic and ground.
3. (Original) The non-inverting domino register of claim 1, wherein said evaluation logic comprises a complex logic circuit.

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4. (Original) The non-inverting domino register of claim 1, wherein said storage stage comprises:
  - a P-channel device having a gate coupled to said pre-charged node and a drain and source coupled between a source voltage and said first preliminary output node;
  - a first N-channel device having a gate receiving said clock signal, a drain coupled to said first preliminary output node and a source; and
  - a second N-channel device having a gate coupled to said pre-charged node, a drain coupled to said source of said first N-channel device and a source coupled to ground.
5. (Original) The non-inverting domino register of claim 4, wherein said keeper circuit comprises a pair of inverters cross-coupled between said first and second preliminary output nodes.
6. (Original) The non-inverting domino register of claim 1, wherein said output stage comprises:
  - a first P-channel device having a gate coupled to said pre-charged node and a drain and source coupled between a source voltage and said output node;
  - a second P-channel device having a gate coupled to said second preliminary output node, a source coupled to said source voltage and a drain coupled to said output node;
  - a first N-channel device having a gate coupled to said second preliminary output node, a drain coupled to said output node and a source; and
  - a second N-channel device having a gate coupled to said pre-charged node, a drain coupled to said source of said first N-channel device and a source coupled to ground.

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7. (Previously Presented) A register, comprising:
  - an evaluation circuit that pre-charges a first node while a clock signal is low and that evaluates a logic function for controlling the state of the first node when said clock signal goes high;
  - a storage circuit, coupled to said first node and receiving said clock signal, that drives a second node high if said first node is low and that drives the second node low if said first node stays high when said clock signal goes high;
  - a keeper circuit, coupled to said second node, that drives a third node to an inverted logic state as said second node; and
  - an output circuit, having a first input coupled to said first node, a second input coupled to said third node and an output coupled to an output node, that drives said output node high if said first or third nodes are low and that drives said output node low if said first and third nodes are both high.
8. (Original) The register of claim 7, wherein said evaluation circuit comprises:
  - a P-channel device, coupled to said first node and receiving said clock signal, that pre-charges said first node while said clock signal is low;
  - a logic circuit, coupled to said first node, that evaluates said logic function based on at least one input data signal; and
  - an N-channel device, coupled to said logic circuit and receiving said clock signal, that enables said logic circuit to evaluate said logic function when said clock signal goes high.
9. (Previously Presented) The register of claim 7, wherein said storage circuit comprises:
  - a P-channel device, coupled to said first and second nodes, that pulls said second node high if said first node goes low;

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a first N-channel device, coupled to said second node and receiving said clock signal; and

a second N-channel device, coupled to said first N-channel device and to said first node;

wherein said first and second N-channel devices collectively pull said second node low if said first node remains high in response to said clock signal going high.

10. (Original) The register of claim 7, wherein said keeper circuit comprises a pair of cross-coupled inverters coupled between said second and third nodes.

11. (Original) The register of claim 7, wherein said output circuit comprises:

a first P-channel device that pulls said output node high when said first node is low;

a second P-channel device that pulls said output node high when said third node is low; and

first and second N-channel devices that collectively pull said output node low when said first and third nodes are both high.

12. (Currently Amended) A method of registering a logic function and generating a non-inverted output signal, comprising:

pre-setting a first node while a clock signal is in a first logic state;

evaluating a logic function to control the logic state of the first node when the clock signal transitions to a second logic state;

driving a second node to an opposite logic state of the first node in response to the clock signal transitioning to its second logic state;

maintaining the second node at its previously driven logic state when the clock signal transitions back to the first logic state from the second logic state;

driving a third node to an opposite logic state of the second node; and

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driving an output node based on the states of the first and third nodes, wherein the output node is driven by an output stage, and wherein the output stage comprises a first pull-up device and a first pull-down device, both responsive to the first node, and a second pull-up device and a second pull-down device, both responsive to the third node.

13. (Original) The method of claim 12, wherein said pre-setting a first node comprises pre-charging the first node to a high logic state.
14. (Original) The method of claim 12, wherein said maintaining the second node at its previously driven logic state comprises coupling a keeper circuit to the second node.
15. (Original) The method of claim 12, wherein said driving a second node comprises:  
pulling the second node high if the first node is low; and  
pulling the second node low if the clock and first nodes are both high.
16. (Original) The method of claim 12, wherein said driving a third node comprises inverting the state of the second node.
17. (Previously Presented) The method of claim 12, wherein said driving an output node comprises:  
pulling the output node high if either of the first and third nodes is low; and  
pulling the output node low if the first and third nodes are both high.